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BRIEF PAPER

The Q-Enhanced CMOS Active Bandpass Filter with Two-Stage Self-Calibration

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SUMMARY A Q-enhanced 8th order CMOS active bandpass filter is presented employing a novel two-stage self-calibration technique. The proposed active filter shows the better out-band attenuation performance than other reported CMOS active bandpass filters. The proposed calibration method enables the stable filtering operation affected by neither the input power variation nor the strong interference power. It is fabricated using 65 nm CMOS process. The measured 3 dB bandwidth is 54 MHz at 2.37 GHz. The insertion loss is 2.9 dB and the out-band attenuation is 27.5 dB at 15 MHz offset frequency. The performance of the filter remains unchanged for ±5% supply voltage variations.

key words: *CMOS bandpass filter, calibration, out-band attenuation*

1. Introduction

The integration of off-chip components in CMOS technology has been one of significant research themes in the design of radio frequency integrated circuits (RFICs) for many years. The CMOS active bandpass-filter (BPF) operating at low GHz frequencies draws considerable attraction since it enables replacement of the off-chip surface acoustic wave (SAW) filter and can be integrated into the CMOS RFIC. This replacement saves the effort for the design of an off-chip matching circuit and minimizes parasitic components caused by off-chip interconnections.

Unfortunately, the low quality (Q) factor of passive components in standard CMOS processes makes it hard to integrate the RF BPF into the RFIC. In addition, it causes the substantial insertion loss in the BPF and low attenuation in the out-band frequency [1].

In this regard, the BPF topology employing active circuits has been proposed since it easily compensates the resistive loss of passive components and raises the Q factor of the BPF [1]–[3]. However, challenges remain with respect to the sharpness and the stability of the BPF.

Up to now, reported active BPFs do not show sufficient out-band attenuation to replace the SAW filter [1]–[3]. Furthermore, conventional calibration techniques have limits to realize the stable operation of the BPF. The conventional calibration techniques are typically classified into two types. Each one is designed to compare the filter output power with either the fixed reference voltage [1], [2] or the input power [4] to control the filter response. However, the filter response can only be controlled under the specific conditions. The first calibration method using the fixed reference voltage loses control when the input power varies beyond the preconditioned range. The second one employing the input power as the reference input would be unstable in strong interference conditions. Large interference power distorts the calibration and makes it difficult to obtain the exact passband characteristics of the BPF.

In this letter, we present the new design technique of the CMOS active BPF to overcome these challenges.

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2. Circuit Design

Figure 1(a) shows the proposed BPF structure. The proposed BPF incorporates the 8th order series-C coupled filter structure for the sufficient out-band attenuation [3]. The CMOS active BPF is composed of two 4th order filter stages. Two filter stages are connected in series. The component values in the LC tank are determined using the following equation.

$$f_{res} = \frac{1}{2\pi\sqrt{LC}} \tag{1}$$

where f_{res}=2.37 GHz. The inductance of 3.76 nH is chosen from the inductor library in the process development kit (PDK) among inductors having Q > 10. The Q factor of the inductor is given by

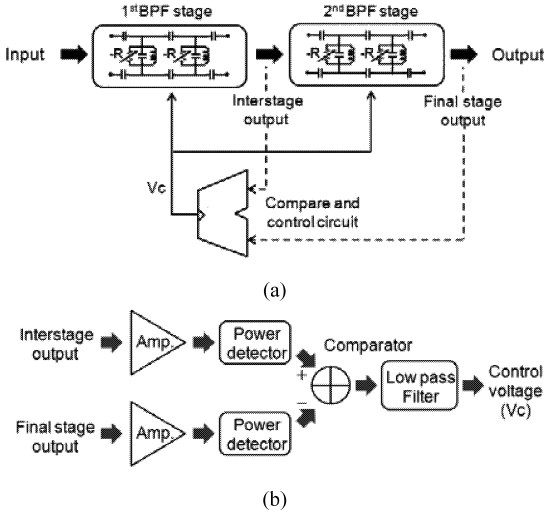

Fig. 1 Block diagram of the proposed filter. (a) The proposed filter structure with two-stage self-calibration. (b) Compare and control circuit.

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$$Q_{ind} = \frac{2\pi \cdot f \cdot L}{R_{para}} \tag{2}$$

where R_{para} means the parasitic resistance of the inductor, and f is the operation frequency. The C value in the tank circuit is correspondingly calculated as 1.2 pF from (1). Considering the parasitic capacitance of CMOS, the capacitor of 0.9 pF was used in the layout. The whole LC tanks in the BPF have the same values of L and C. The series coupling capacitor (C_{series}) between LC tanks is empirically found to be 30 fF. The LC tank is realized in the PMOS-NMOS cross-coupled pair in Fig. 2. The cross-coupled pair generates a negative resistance (-R, see Fig. 1(a)), which effectively removes the parasitic resistance of the LC tank. By changing an applied voltage (V_c) in the current source, the magnitude of the negative resistance can be controlled. The control voltage can be found as below,

$$V_c = P_{in} \cdot L_1 \cdot A - P_{in} \cdot L_1 \cdot L_2 \cdot A \tag{3}$$

where L_1 and L_2 are the gain of the first and second stage filter, A is the amplifier gain, and P_{in} is the input power. This control scheme affects the performance of the 4th order active BPF and enables the feedback loop to modulate the negative resistance. The sizes of transistors are optimized to compensate the parasitic resistance and give a high Q value of 50 in the LC tank.

The proposed CMOS active BPF employs a novel two-stage self-calibration technique for the stable operation. The major part of the two-stage self-calibration technique is the control voltage generation by incorporating the feedback loop. In the feedback loop, the V_c varies to regulate the filter characteristic and saturates to the certain level by the negative feedback. The feedback loop for the calibration is composed of the comparator and control circuit (CCC) (see Fig. 1(b)). The self-calibration is executed by comparing the powers from the outputs of the 1st and the 2nd filter stage and generating V_c. The interstage output obtained at the output of the first 4th order filter is amplified and converted into the corresponding power level in the power detector [5]. And, the output of the 2nd filter stage is also processed in the same way. These two signals are then compared in the comparator circuit. The low pass filter (LPF) follows the comparator. It stabilizes the feedback loop by regulating the loop bandwidth.

When the input power changes rapidly, each output of the interstage and the final stage can track the input power variation. In addition, the precise pass-band response of the BPF can be detected even under the strong interference condition. This is because both the interstage and the final stage output are already filtered out and contain sufficiently small amount of the interference signal not to distort the comparison result.

The CCC loop is configured to output the control signal with the proper DC level [5]. The control signal (V_c) drives the current source of the 1st and the 2nd filter stage. When the V_c increases, the larger current flows in the cross-coupled pair. This causes larger negative resistance in the circuit and results in larger pass-band gain. In the opposite case, while the filter shows unstable response, the CCC decreases the V_c. This causes the reduction of the negative resistance and leads to the lower pass-band gain. This feedback operation with the CCC stabilizes the pass-band response of the filter.

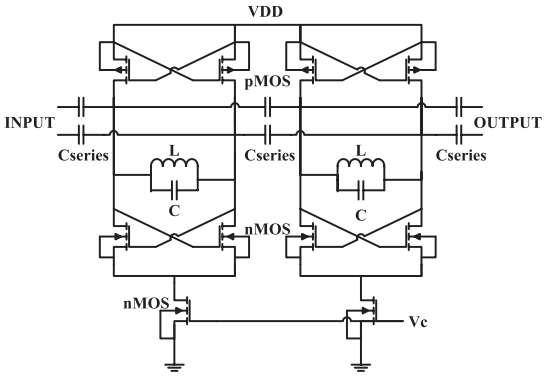

Fig. 2 The 4th order active BPF structure with PMOS-NMOS cross-coupled pair.

3. Experiment

The proposed BPF is fabricated using 65 nm CMOS process and its photograph is shown in Fig. 3. The measured 3 dB bandwidth is 54 MHz at 2.37 GHz center frequency.

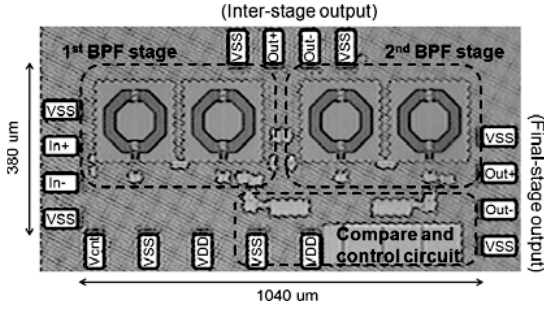

Fig. 3 Die photo of the proposed filter ($1040 \times 380\,\mu m^2$).

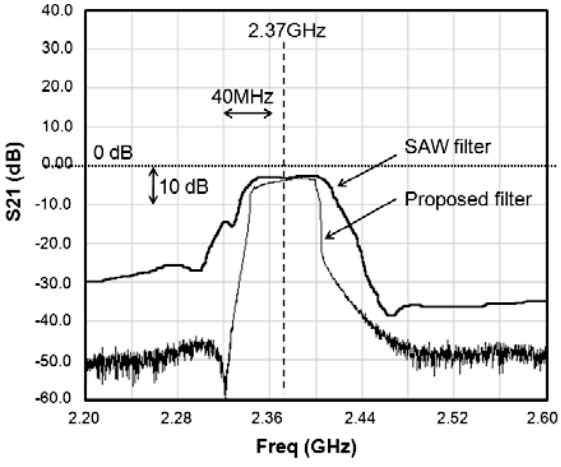

Fig. 4 Measured S_{21} of the proposed filter and the SAW filter.

It shows the insertion loss of 2.9 dB. The out-band attenuation is 27.5 dB at 15 MHz offset. It is even higher attenuation than the off-chip SAW filter. Figure 4 shows the graphical comparison of the proposed CMOS active BPF with the commercial SAW filter (Oscillent 802-RF2375.0M-A). The measured attenuation characteristic of the proposed CMOS BPF is remarkably sharp compared to the SAW device. The measured noise figure is 17–19 dB in the passband. In addition, we demonstrate that the proposed two-stage self-calibration technique enables the filter to be stable for ±5% supply voltage variation (Fig. 5). Without the calibration loop, the filter shows the different and unstable results depending on the supply voltage as shown in Fig. 5(a). However, after turning on the calibration loop, the S_{21} remains unchanged regardless of the supply voltage (see Fig. 5(b)). This comparison result validates that the proposed two-stage self-calibration with the CCC successfully stabilizes the CMOS active BPF. The two-tone test shows the in-band 3rd order input intercept point (IIP3) of −12.5 dBm as given in Fig. 6. The entire circuit including both the filter and the CCC consumes 18 mA under 1.45 V supply voltage. It occupies an area of $1040 \times 380\,\mu m^2$ excluding PADs. The performance summary and the comparison with other works are shown in Table 1. It reveals that the proposed BPF is superior to others in terms of the out-band attenuation.

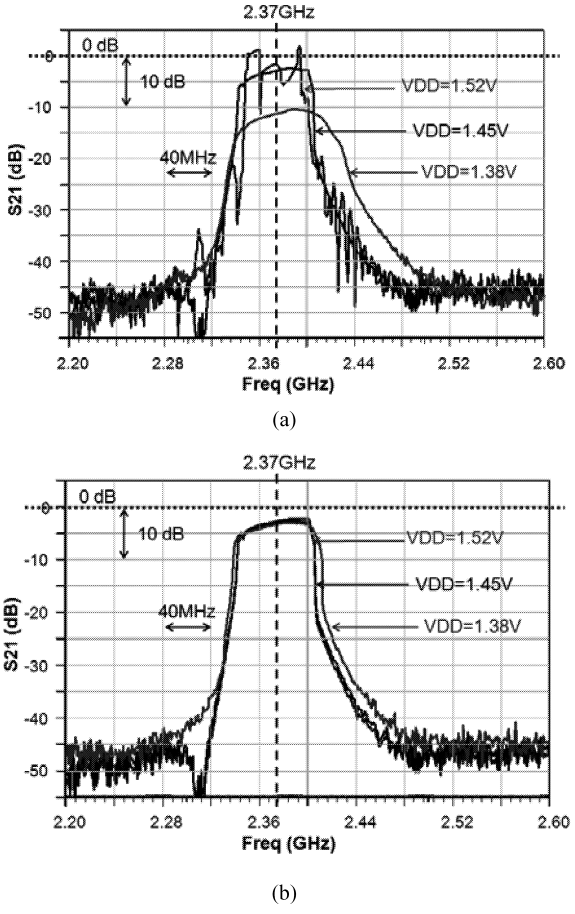

Fig. 5 Measured S_{21} of the proposed filter for supply voltage variations. (a) Turning off the calibration. (b) Turning on the self-calibration loop.

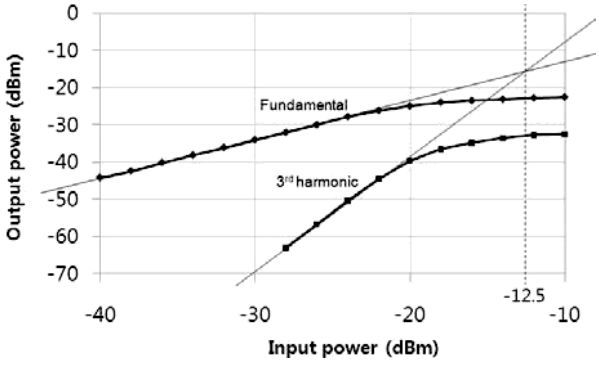

Fig. 6 Measured IIP3 of the proposed CMOS active BPF.

Table 1 Performance comparisons of reported CMOS active BPFs.

	Unit	This work	[1]	[2]	[3]	[4]
Process	nm	65	250	180	180	180
Filter Order	-	8	6	4	6	4
Center Frequency	GHz	2.37	2.14	2.03	2.36	6.1
3 dB bandwidth	MHz	54	60	130	60	100
DC power	mW	26.1	17.5	16.6	8.8	-
NF	dB	17	-	15	19	-
IIP3	dBm	-12.5	-4.9	2.5	-8.5	-
Out-band attenuation (offset freq.)	dB (MHz)	27.5 (15)	24 (210)	17 (100)	30 (100)	15 (100)
Calibration	-	2-stage self-calibration	Fixed voltage	Fixed voltage	-	Input power

4. Results and Discussions

We implemented and measured the proposed 8th order CMOS active BPF which shows remarkable out-band attenuation of 27.5 dB at 15 MHz offset. This result surpasses that of the SAW filter. Also, the proposed two-stage self-calibration enables the stable operation of the BPF. By carrying out the calibration in the feedback loop, it solves the calibration problems caused by the input power variation or the strong interference. To the authors' knowledge, the proposed self-calibration technique is firstly proposed and experimentally demonstrated. It is anticipated that the proposed active BPF would replace the SAW component and play a key role in realizing the SAW-less RFIC.

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